Notes on usage of 24-bit SPI port expansion boards from AliExpress:

74HC165 Key Expansion Board Shift Register
24 bits input, SPI bus out, cascadable

4.7 13 Reviews | 92 sold

AU$6.21 29% off ~~AU$8.74~~

Tax excluded, add at checkout if applicable

AU$3.00 off on AU$23.00

Color: 1PCS


The boards are well made and they come with hookup wires and plugs for all connectors. However, the colour-coding of the wires is contrary to convention. Each of the 6 input pin headers has one pin routed to GND. The matching plugs have a black wire which you might expect to connect to the GND pin, but in fact the black wires connect to input signals!

If the wire colour scheme bothers you, it's not too difficult to remove the wires from the plugs to rearrange them. Using a small jewellers screw-driver (flat blade), carefully lift the tiny plastic tab holding the crimp contact in place. The barb on the contact should slide under the tab allowing the contact to be removed when the wire is pulled gently.

The schematic downloaded from the supplier is misleading and contains errors.

The connector marked "IN" on the schematic and on the PCB is in fact a "carry" output to a lower-order cascaded board, or to the micro-controller SPI master input (MISO), so really it should be marked "OUT". Likewise, the connector marked "OUT" is in fact a "carry" input from a higher-order cascaded board. The signal routed from the "OUT" connector to U3 pin-10 is an input, misleadingly marked 'Data_9' on both "IN" and "OUT" connectors on the PCB!

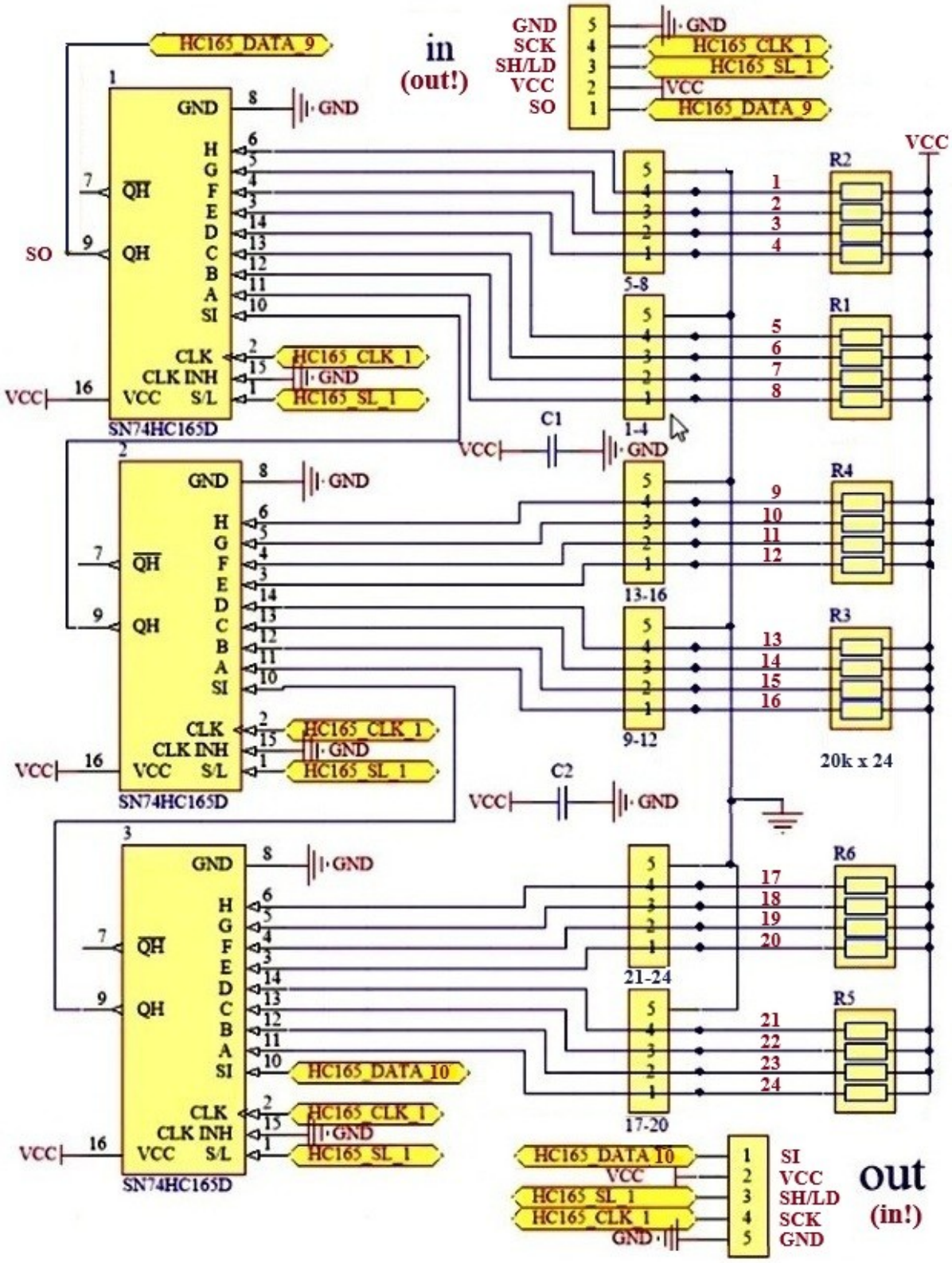
The schematic shows resistors connected from the 24 input pins to GND. In fact, the resistors are connected to VCC (+5V) to act as pull-ups, as required. The resistors are designated "103" (i.e. 10k), whereas the resistors fitted on the board are actually 20k.

Following is a corrected version of the schematic, marked according to the actual circuit (as built), and with input pins renumbered sequentially (1 ~ 48) for use with SPI transfer mode "LSB first". Corrected signal labels are written in dark red text.

SPI clocking and transfer modes:

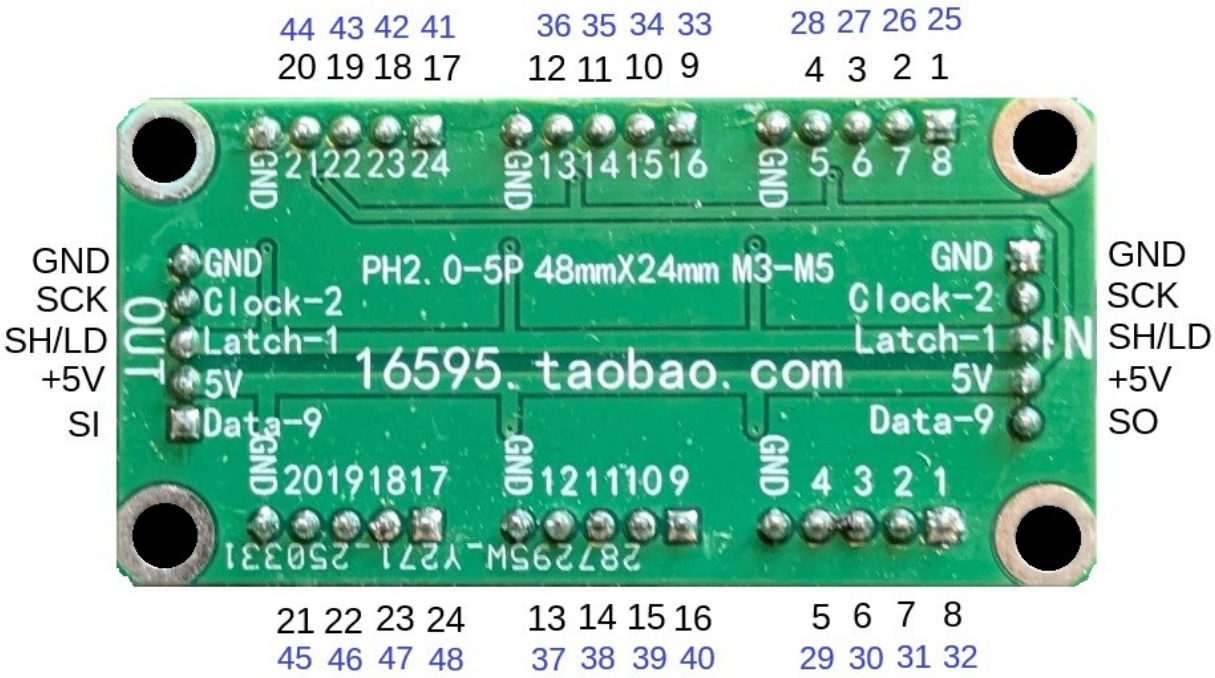
Input pins were labelled on the assumption that the SPI transfer mode is "MSB first", i.e. pin '8' is the MSB (bit 7) of the first byte transferred. Since stage 'H' of the 74HC165 is shifted out first, and the serial input (SI) is a "carry in" from the next (higher-order) register, it seems more logical to regard stage 'H' as the LS bit and to use SPI transfer mode "LSB first".

The port expander pins should be re-labelled so that the 'HC165 stage 'H' is the lowest numbered input of each 8-bit register, if using SPI mode "LSB first" (recommended).



When the signal SH/LD is Low, parallel input data are loaded into the registers. When SH/LD is High, the data bits are shifted out serially via SO (= MISO). SH/LD must remain High during transfer of all 24 (or 25) bits. Refer to the 74HC165 data-sheet for further information.

24-BIT SPI INPUT PORT EXPANDER -- PINOUT (MSB FIRST)



The alternative pin numbering scheme shown above and below the board applies to SPI transfer mode “LSB first”. The blue pin numbers apply to a second (higher-order) cascaded board, if any.

Note that the serial input (SI) may be used to provide a 25th input signal. This will appear in all bits of the 4th byte transferred via SPI. The highest-order cascaded board should have its serial input (SI) tied to VCC if it is not used as an extra input bit.